IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Canceled).

2. (Currently Amended) A system for verifying ~~a design element~~ integrated circuit logic of a system-on-a-chip (SOC) ~~design~~, said system comprising:

an SOC comprising:

~~said design element;~~

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said ~~design element~~ integrated circuit logic in response to running a verification case;

an SOC interface that receives said second set of signals; and

a first external bus interface unit (EBIU) that is slaved to said master CPU and receives said first set of signals; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification ~~logic device~~ interface model connected to said SOC interface; and

a second EBIU connected to said first EBIU and to said verification ~~logic device~~ interface model;

wherein said first set of signals received by said second EBIU is inputted to said verification ~~logic device~~ interface model and said verification interface model outputs data for said verification case to said SOC interface; and

wherein said verification case checks for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals and records a verification case status ~~second set of signals received from said SOC is inputted to said verification logic device; and~~

~~wherein said verification logic device verifies said design element integrated circuit logic based on inputs from said first set of signals and said second set of signals~~.

3-7. (Canceled).

8. (Currently Amended) A system for verifying ~~a design element~~ integrated circuit logic of a system-on-a-chip (SOC) ~~design~~, said system comprising:

an SOC comprising:

~~said design element;~~

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said ~~design element~~ integrated circuit logic in response to signals produced by running a verification case;

an SOC interface that receives said second set of signals, said SOC interface being connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification ~~logic device~~ interface model connected to said SOC interface by a second external bus; and

a second EBIU connected to said first EBIU by a first external bus and to said verification ~~logic device~~ interface model by a third internal bus;

wherein said first set of signals received by said second EBIU is inputted to said verification ~~logic device~~ interface model via said third internal bus and said verification interface model outputs data for said verification case to said SOC interface via said data bus; and

wherein said verification case checks for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals via said

first internal bus and records a verification case status ~~second set of signals received from said SOC interface via said second external bus is inputted to said verification logic device; and~~

~~wherein said verification logic device verifies said design element based on inputs from said first set of signals and said second set of signals~~.

9. (Previously Presented) The system in claim 8, wherein said verification case comprises software drivers.

10. (Currently Amended) The system in claim 8, wherein registers of said SOC interface and said verification ~~logic device~~ interface model are controlled by the same verification case.

11. (Currently Amended) The system in claim 10, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification ~~logic device~~ interface model.

12. (Currently Amended) The system in claim 10, wherein said verification ~~test~~ case utilizes different software drivers to configure and control said SOC interface and said verification ~~logic device~~ interface model.

13. (Currently Amended) The system in claim 8, wherein said verification ~~logic device~~ interface model tests an operational capability of said SOC interface.

14. (Currently Amended) The system in claim 8, further comprising an additional verification ~~logic device~~ interface model for said verification test bench, said additional verification ~~logic device~~ interface model being connected to said second EBIU for testing additional types of SOC interfaces.

15. (Currently Amended) A system for verifying ~~a design element~~ integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising:

~~said design element;~~

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said ~~design element~~ integrated circuit logic in response to signals produced by running a verification case;

an SOC interface that receives said second set of signals, said SOC interface being connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification ~~logic device~~ interface model connected to said SOC interface by a second external bus; and

a second EBIU connected to said first EBIU by a first external bus and to said verification ~~logic device~~ interface model by a third internal bus;

wherein said second EBIU and said first EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said verification ~~logic device~~ interface model receive said first set of signals and said second set of signals, respectively, as inputs based on the running of said verification case by said master CPU; and

wherein said verification ~~logic device verifies said design element based on said inputs from said first set of signals and said second set of signals~~ case checks for correctness of outputted data from said verification interface model to said SOC interface by said second set of signals and records a verification status.

16. (Previously Presented) The system in claim 15, wherein said verification case comprises software drivers.

17. (Currently Amended) The system in claim 15, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification ~~logic device~~ interface model.

18. (Currently Amended) The system in claim 15, wherein verification test case utilizes different software drivers to configure and control said SOC interface and said verification ~~logic device~~ interface model.

19. (Currently Amended) The system in claim 15, wherein said verification ~~logic device~~ interface model tests an operational capability of said SOC interface.

20. (Currently Amended) The system in claim 15, further comprising an additional verification ~~logic device~~ interface model for said verification test bench, said additional verification ~~logic device~~ interface model being connected to said second EBIU for testing additional types of SOC interfaces.

21. (Currently Amended) A method for verifying ~~a design element~~ integrated circuit logic of a system-on-a-chip (SOC) ~~design~~, said method comprising:

producing a first set of signals and a second set of signals by a master central processing unit (CPU) of an SOC, which includes said ~~design element~~ integrated circuit logic, in response to running a verification case on said master CPU;

slaving an SOC interface, which receives said second set of signals, and a first external bus interface unit (EBIU) of said SOC, which receives said first set of signals, to said master CPU of said SOC;

connecting said SOC interface to an external verification ~~logic device~~ interface model, which is external to said SOC;

connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU being connected to said external verification ~~logic device~~ interface model;

inputting said first set of signals, received by said second EBIU, into said verification ~~logic device~~ interface model;

inputting said second set of signals, received by ~~from~~ said SOC interface~~, into said verification logic device~~; and

verifying said ~~design element based on inputs from said first set of signals and said second set of signals to said verification logic device~~ verification case by checking for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals and recording a verification case status.

22. (Previously Presented) The method in claim 21, wherein said verification case comprises software drivers.

23. (Currently Amended) The method in claim 21, further comprising controlling registers of said SOC interface and said verification ~~logic device~~ interface model by the running of the verification case on the master CPU.

24. (Currently Amended) The method in claim 23, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification ~~logic device~~ interface model.

25. (Currently Amended) The method in claim 23, wherein said verification case utilizes different software drivers to configure and control said SOC interface and said verification ~~logic device~~ interface model.

26. (Currently Amended) The method in claim 21, further comprising comparing said [[said]] first set of signals, received by said second EBIU, and inputted into said verification ~~logic device~~ interface model and said second set of signals, received ~~by~~ from said SOC interface, and inputted into said verification ~~logic device~~ interface model to test an operational capability of said SOC interface.

27. (Currently Amended) The method in claim 21, further comprising:

connecting at least one additional verification ~~logic device~~ interface model to said second EBIU; and

testing additional types of SOC interfaces.

28-34. (Canceled).